Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

Claims 1-26 (Cancelled).

27. (New) A first-in-first-out (FIFO) data system, comprising:

a FIFO memory that has a binary write point input, a binary read pointer input, a write data input, a write clock input, and a read data output, wherein the FIFO memory comprises a data structure of depth d from which data may be written into using the write data input and read out using the read data output, wherein d is not a value of 2^n in which d and n are integers;

an output of a first set of flip flops coupled to an input of a first gray-to-binary converter, an input of a first gray-code generator, an input of a second set of flip flops, and an input of write clock logic that generates a first empty signal, a first full signal, and a first almost full signal;

an output of the first gray-to-binary converter coupled to the binary write pointer input;

an output of the first gray-code generator coupled to an input of the first set of flip flops;

the output of the second set of flip flops coupled to an input of read clock logic that generates a second empty signal, a second full signal, and a second almost full signal;

an output of a third set of flip flops coupled to an input of a second gray-to-binary converter, an input of a second gray-code generator, an input of a fourth set of flip flops, and an input of the read clock logic;

an output of the second gray-code generator coupled to an input of the third set of flip flops;

an output of the second gray-to-binary converter coupled to the binary read pointer input; and

an output of the fourth set of flip flops coupled to the input of the write clock logic.

28. (New) The FIFO data system according to claim 27, comprising:

a read clock; and

a write clock,

wherein the read clock and the write clock do not have a phase relationship.

29. (New) The FIFO data system according to claim 27, comprising:

a read clock; and

a write clock,

wherein the read clock and the write clock do not have a periodic time relationship.

30. (New) The FIFO data system according to claim 27, comprising:

a read clock; and

a write clock,

wherein the read clock and the write clock are asynchronous.

31. (New) The FIFO data system according to claim 27,

wherein the first set of flip flops, the fourth set of flip flops, the first gray-to-binary converter, the first gray-code generator and the write clock logic are part of a write clock domain, wherein the second set of flip flops, the third set of flip flops, the second gray-to-binary converter, the second gray-code generator and the read clock logic are part of a write clock domain, and wherein the FIFO memory is part of both the write clock domain and the read clock domain.

32. (New) The FIFO data system according to claim 31, wherein the fourth set of flip flops are configured to synchronize the third set of flip flops into the write clock domain.

33. (New) The FIFO data system according to claim 31, wherein the second set of flip slops are configured to synchronize the first set of flip flops into the read clock domain.

34. (New) The FIFO data system according to claim 27, wherein the FIFO data system provides resilience towards meta-stability situations.

35. (New) The FIFO data system according to claim 27, wherein the second set of flip flops transmit gray codes.

36. (New) The FIFO data system according to claim 35, wherein the fourth set of flip flops transmit gray codes.

37. (New) The FIFO data system according to claim 27, wherein the second set of flip flops and the fourth set of flip flops are part of a synchronization system that guarantees that a meta-stability resolution time is less than a period of a receiving clock.

38. (New) The FIFO data system according to claim 27, wherein the first gray-code generator generates a first gray-code sequence, wherein the first gray-code generator reduces the first gray-code sequence into a second gray-code sequence by removing one or more pairs of gray codes from the first gray-code sequence.

39. (New) The FIFO data system according to claim 38, wherein each gray code of the first-gray code sequence has m bits, wherein m is an integer, wherein each removed pair of gray-codes comprises a first m-bit gray code and a second m-bit gray code, and wherein the first m-bit gray code and the second m-bit gray code of a respective removed pair have the same m-1 least significant bits.

40. (New) The FIFO data system according to claim 38, wherein each of the one or more pairs of gray codes removed from the first gray-code sequence comprises two gray codes that differ only by their respective most significant bits.

41. (New) The FIFO data system according to claim 27, wherein the first gray-to-binary converter receives a gray-code sequence that has been reduced by removing pairs of gray codes, each removed gray-code pair comprises respective gray codes that differ only by their respective most significant bits.

42. (New) The FIFO data system according to claim 27, wherein the first gray-to-binary converter receives a gray-code sequence that has been reduced by removing pairs of gray codes, each removed gray-code pair comprises respective m-bit gray codes that have the same m-1 least significant bits, and wherein m is an integer.

43. (New) The FIFO data system according to claim 27, wherein the FIFO data system is part of a very large scale integration (VLSI).

44. (New) The FIFO data system according to claim 27, wherein the FIFO data system is an asynchronous FIFO data system.